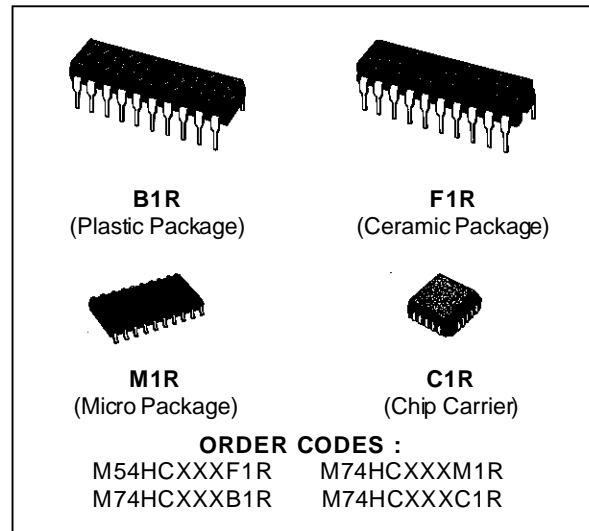


OCTAL BUS TRANSCEIVER (3-STATE): HC245 NON INVERTING HC640 INVERTING, HC643 INVERTING/NON INVERTING

- HIGH SPEED
 $t_{PD} = 10 \text{ ns (TYP.) at } V_{CC} = 5\text{V}$
- LOW POWER DISSIPATION
 $I_{CC} = 4 \mu\text{A (MAX.) at } T_A = 25^\circ\text{C}$
- HIGH NOISE IMMUNITY
 $V_{NIH} = V_{INL} = 28\% V_{CC} \text{ (MIN.)}$
- OUTPUT DRIVE CAPABILITY
15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
 $|I_{OH}| = I_{OL} = 6 \text{ mA (MIN)}$
- BALANCED PROPAGATION DELAYS
 $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
 $V_{CC} \text{ (OPR)} = 2 \text{ V TO } 6 \text{ V}$
- PIN AND FUNCTION COMPATIBLE
WITH 54/74LS245/640/643



DESCRIPTION

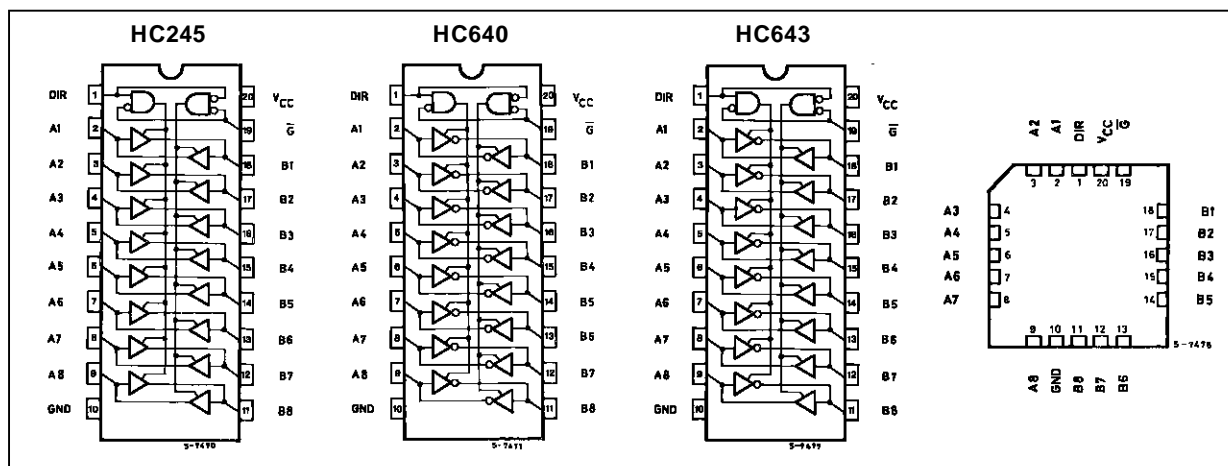
The M54/74HC245, HC640 and HC643 utilise silicon gate C²MOS technology to achieve operating speeds equivalent to LSTTL devices.

Along with the low power dissipation and high noise immunity of standard C²MOS integrated circuit, it possesses the capability to drive 15 LSTTL loads. These IC's are intended for two-way asynchronous communication between data buses, and the direction of data transmission is determined by DIR input. The enable input (\bar{G}) can be used to disable the device so that the buses are effectively isolated.

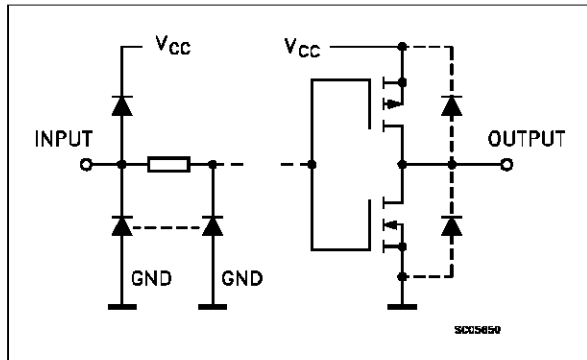
All inputs are equipped with protection circuits against static discharge and transient discharge and transient excess voltage.

IT IS PROHIBITED TO APPLY A SIGNAL TO A BUS TERMINAL WHEN IT IS IN OUTPUT MODE AND WHEN A BUS TERMINAL IS FLOATING (HIGH IMPEDANCE STATE), IT IS REQUESTED TO FIX THE INPUT LEVEL BY MEANS OF EXTERNAL PULL DOWN OR PULL UP RESISTOR.

PIN CONNECTION (top view)



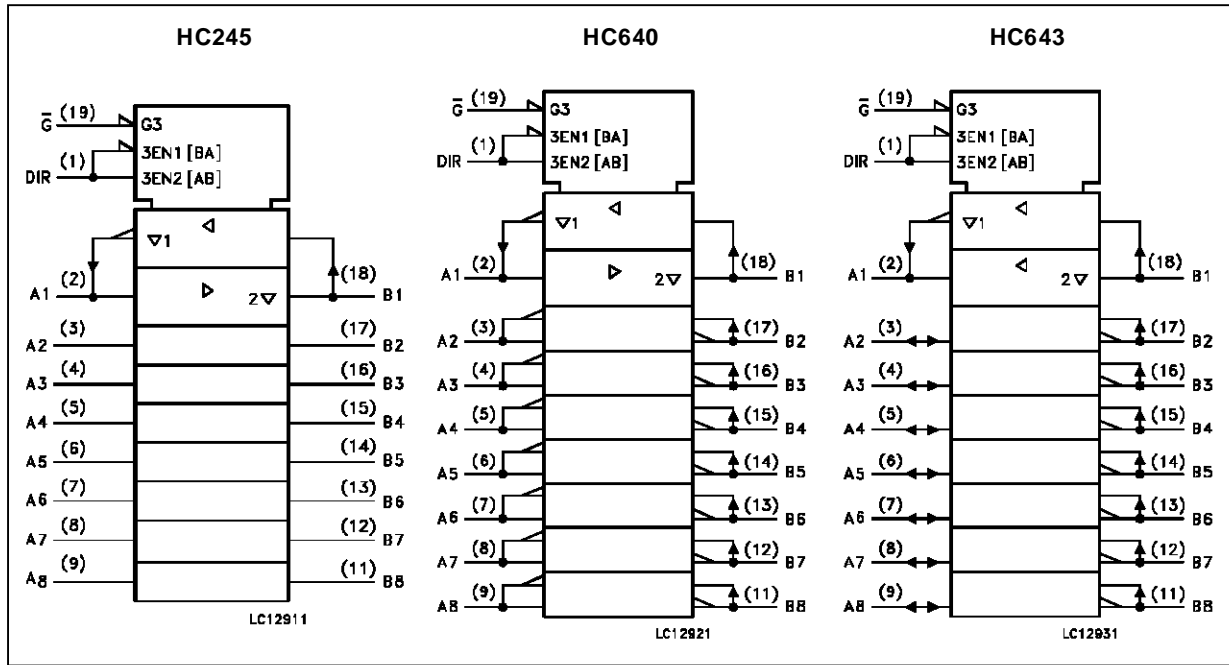
INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	DIR	Directional Control
2, 3, 4, 5, 6, 7, 8, 9	A1 to A8	Data Inputs/Outputs
18, 17, 16, 15, 14, 13, 12, 11	B1 to B8	Data Inputs/Outputs
19	\overline{G}	Output Enable Input (Active LOW)
10	GND	Ground (0V)
20	V _{CC}	Positive Supply Voltage

IEC LOGIC SYMBOLS

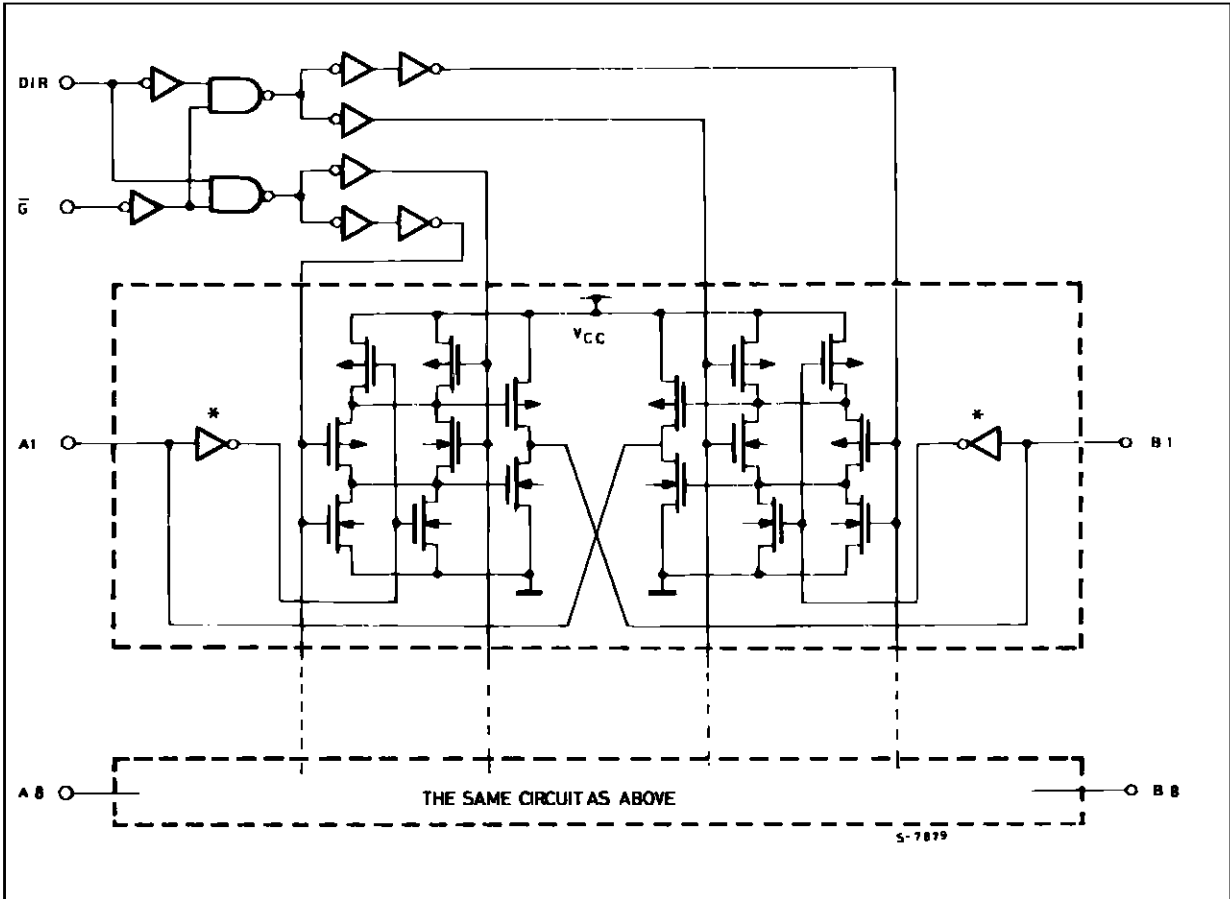


TRUTH TABLE

INPUT		FUNCTION		OUTPUT		
\overline{G}	DIR	A BUS	B BUS	HC245	HC640	HC643
L	L	OUTPUT	INPUT	A = B	A = \overline{B}	A = B
L	H	INPUT	OUTPUT	B = A	B = \overline{A}	B = \overline{A}
H	X	Z	Z	Z	Z	Z

X: "H" or "L"
Z: High impedance

LOGIC DIAGRAM (HC640)



NOTE: IN CASE OF HC245 OR HC643, INPUT INVERTERS MARKED* AT A BUS AND B BUS ARE ELIMINATED RESPECTIVELY

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	-0.5 to +7	V
V _I	DC Input Voltage	-0.5 to V _{CC} + 0.5	V
V _O	DC Output Voltage	-0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	± 20	mA
I _{OK}	DC Output Diode Current	± 20	mA
I _O	DC Output Source Sink Current Per Output Pin	± 35	mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current	± 70	mA
P _D	Power Dissipation	500 (*)	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
 (*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit	
V _{CC}	Supply Voltage	2 to 6	V	
V _I	Input Voltage	0 to V _{CC}	V	
V _O	Output Voltage	0 to V _{CC}	V	
T _{op}	Operating Temperature: M54HC Series M74HC Series	-55 to +125 -40 to +85	°C °C	
t _r , t _f	Input Rise and Fall Time	V _{CC} = 2 V	0 to 1000	ns
		V _{CC} = 4.5 V	0 to 500	
		V _{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

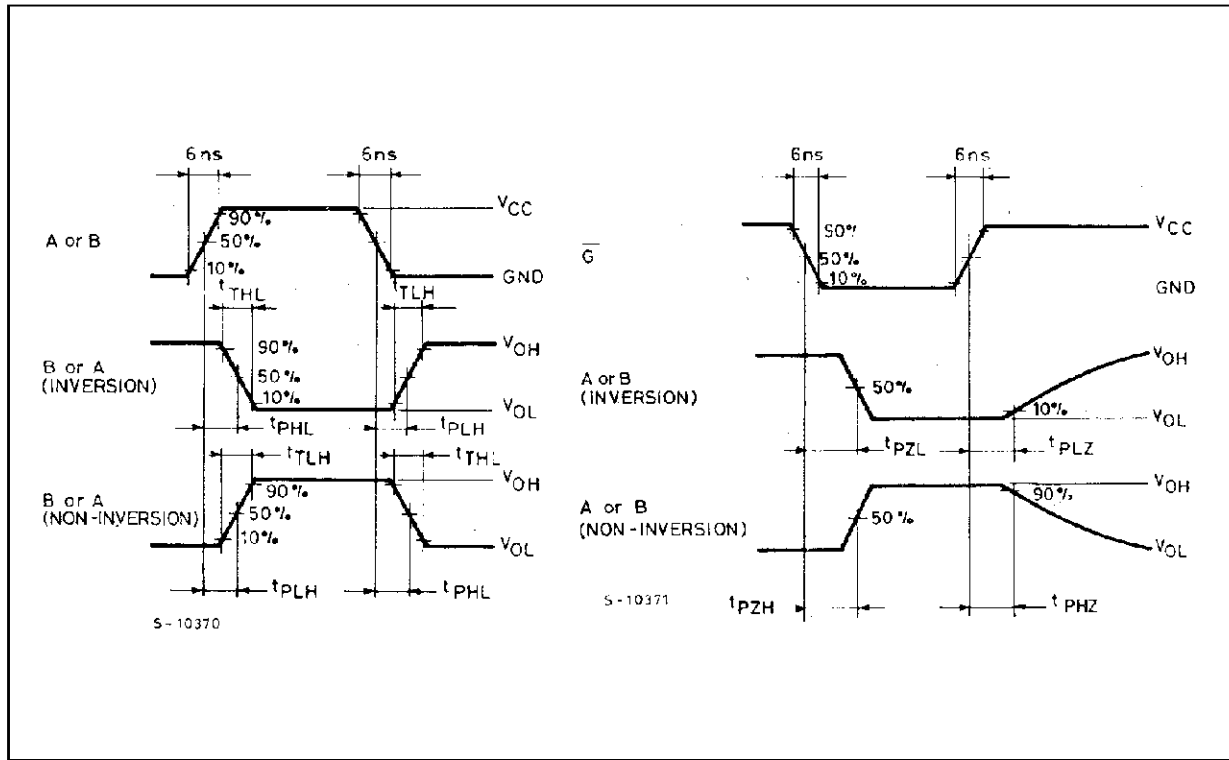
Symbol	Parameter	Test Conditions		Value						Unit							
				T _A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC								
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.						
V _{IH}	High Level Input Voltage	V _{CC} (V)								V							
		2.0									1.5			1.5		1.5	
		4.5									3.15			3.15		3.15	
V _{IL}	Low Level Input Voltage	V _{CC} (V)								V							
		2.0											0.5		0.5		0.5
		4.5											1.35		1.35		1.35
V _{OH}	High Level Output Voltage	V _{CC} (V)	V _I = V _{IH} or V _{IL}	I _O = -20 μA						V							
		2.0									1.9	2.0		1.9		1.9	
		4.5									4.4	4.5		4.4		4.4	
V _{OL}	Low Level Output Voltage	V _{CC} (V)	V _I = V _{IH} or V _{IL}	I _O = 20 μA						V							
		2.0										0.0	0.1		0.1		0.1
		4.5										0.0	0.1		0.1		0.1
I _I	Input Leakage Current	V _{CC} (V)	V _I = V _{CC} or GND							μA							
		2.0											±0.1		±1		±1
		4.5											±0.5		±5.0		μA
I _{CC}	Quiescent Supply Current	V _{CC} (V)	V _I = V _{CC} or GND							μA							
		2.0											4		40		80
		4.5															

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

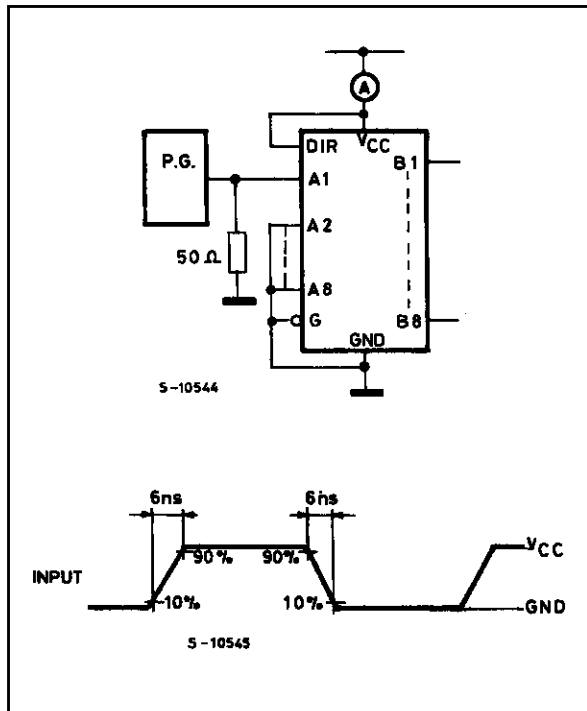
Symbol	Parameter	Test Conditions			Value						Unit		
		V _{CC} (V)	C _L (pF)		T _A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC			
					Min.	Typ.	Max.	Min.	Max.	Min.		Max.	
t _{TLH} t _{THL}	Output Transition Time	2.0	50			25	60		75		90	ns	
		4.5				7	12		19		18		
		6.0				6	10		13		15		
t _{PLH} t _{PHL}	Propagation Delay Time	2.0	50			33	90		115		135	ns	
		4.5				12	18		23		27		
		6.0				10	15		20		23		
		2.0	150			48	120		150		180	ns	
		4.5				16	24		30		36		
		6.0				14	20		26		31		
t _{PZL} t _{PZH}	Output Enable Time	2.0	50	R _L = 1KΩ		48	150		190		225	ns	
		4.5					16	30		38			45
		6.0					14	26		32			38
		2.0	150	R _L = 1KΩ		63	180		225		270	ns	
		4.5					21	36		45			54
		6.0					18	31		38			46
t _{PLZ} t _{PHZ}	Output Disable Time	2.0	50	R _L = 1KΩ		37	150		190		225	ns	
		4.5					17	30		38			45
		6.0					15	26		32			38
C _{IN}	Input Capacitance			DIR, \overline{G}		5	10		10		10	pF	
C _{I/OUT}	Output Capacitance			An, Bn		13						pF	
C _{PD} (*)	Power Dissipation Capacitance			HC245 HC640/643		39 37						pF	

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. I_{cc(opr)} = C_{PD} • V_{CC} • f_{IN} + I_{cc}/8 (per circuit)

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)



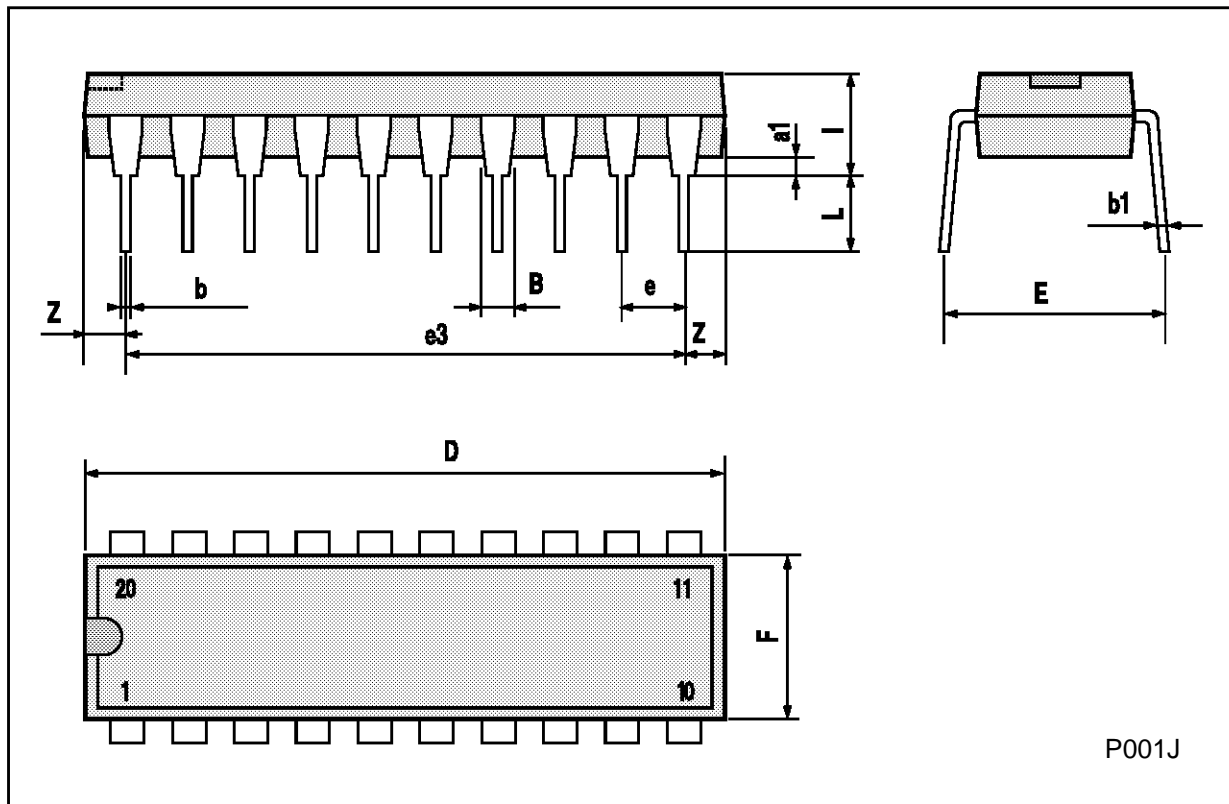
C_{PD} CALCULATION

C_{PD} is to be calculated with the following formula by using the measured value of I_{CC} (Opr.) in the test circuit opposite.

$$C_{PD} = \frac{I_{CC} (Opr.)}{f_{IN} \times V_{CC}}$$

Plastic DIP20 (0.25) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053



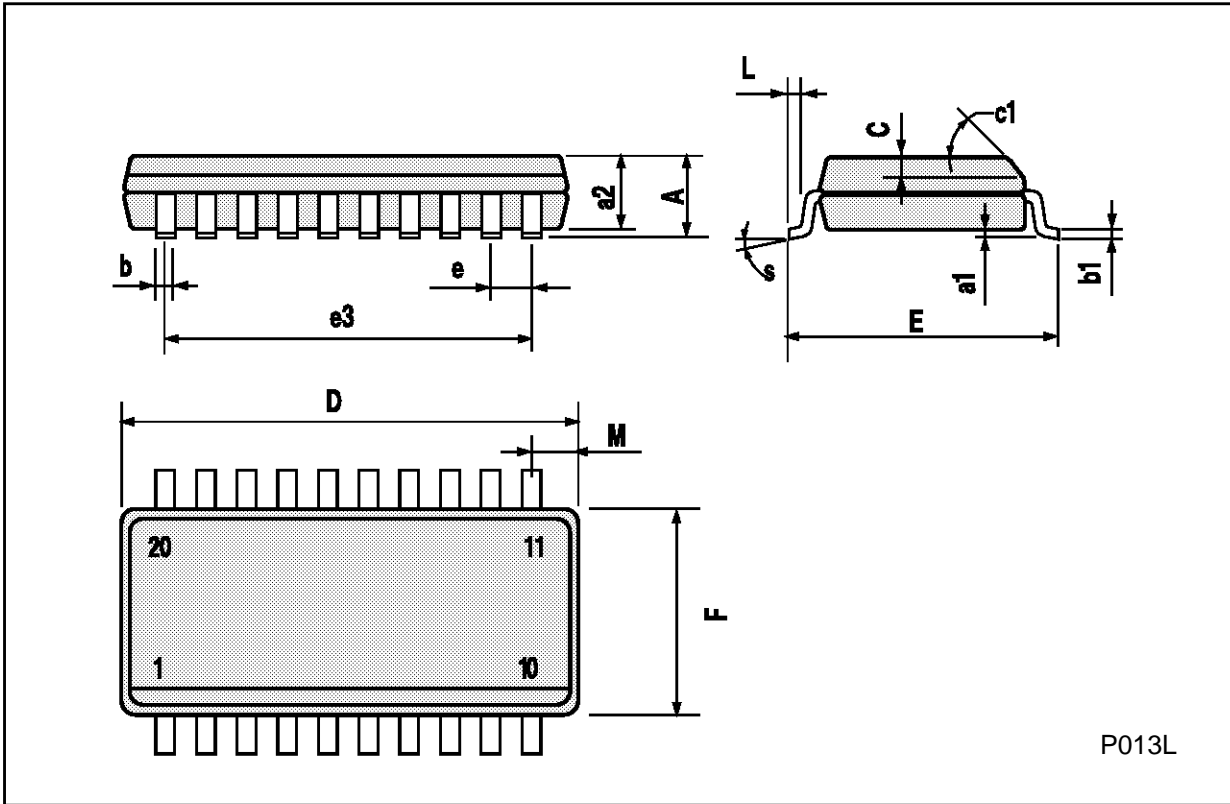
Ceramic DIP20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			25			0.984
B			7.8			0.307
D		3.3			0.130	
E	0.5		1.78	0.020		0.070
e3		22.86			0.900	
F	2.29		2.79	0.090		0.110
G	0.4		0.55	0.016		0.022
I	1.27		1.52	0.050		0.060
L	0.22		0.31	0.009		0.012
M	0.51		1.27	0.020		0.050
N1	4° (min.), 15° (max.)					
P	7.9		8.13	0.311		0.320
Q			5.71			0.225



SO20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.10		0.20	0.004		0.007
a2			2.45			0.096
b	0.35		0.49	0.013		0.019
b1	0.23		0.32	0.009		0.012
C		0.50			0.020	
c1	45° (typ.)					
D	12.60		13.00	0.496		0.512
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.40		7.60	0.291		0.299
L	0.50		1.27	0.19		0.050
M			0.75			0.029
S	8° (max.)					



P013L

PLCC20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	9.78		10.03	0.385		0.395
B	8.89		9.04	0.350		0.356
D	4.2		4.57	0.165		0.180
d1		2.54			0.100	
d2		0.56			0.022	
E	7.37		8.38	0.290		0.330
e		1.27			0.050	
e3		5.08			0.200	
F		0.38			0.015	
G			0.101			0.004
M		1.27			0.050	
M1		1.14			0.045	



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